MY-Semi

Preliminary

# MY9942

## 4 Channels Constant Current LED Driver With Addressable DMX512 Protocol and Differential Interface

## General Description

The MY9942, 4 channels constant current LED driver with 14bits grayscale APDM (Adaptive Pulse Density Modulation) control, supports standard / 4X DMX512 protocol and fully differential interface suited for long distance parallel applications. The distinctive DMX512 decoding approach could decode precisely a standard DMX512 signal. And each device loads one/two/three/four grayscale data according to two slot selection pins and nine address setting pins (512 addresses). The differential interface provides wide common-mode range to support long distance transmission without common-ground power systems.

The device operates over 7V to 40V input voltage range and provides 4 open-drain constant current sinking outputs that are rated to 50V and delivers up to 350mA of high accuracy current to each string of LED. The current at each output is programmable by means of four external current setting resistors. The MY9942 provides the gamma correction, gamma value is 2.2, to transform 8bits DMX data to 14bits APDM data in order to enhance brightness contract. The 14bits adaptive pulse density modulation makes sure that the frame refresh rate is higher than 2KHz. And an accurate oscillator is built in for free running APDM grayscale control and DMX512 decoder.

Furthermore, MY9942 could drive High Power LED directly by shorting the output channels and changing the slot data number. The POL function makes MY9942 as a PWM generator to support driving high power LEDs. MY9942 is available in 28-pin SSOP/TSSOP packages and specified over the -40°C to +85°C ambient temperature range.

## Features

- **White / CW.WW / R.G.B / R.G.B.W applications**
- **One / Two / Three / Four slots data selection for different LED configuration applications**
- **7V to 40V Operating supply voltage**
- **350mA maximum constant current output (Per channel)**
- **Current setting by 4 external resistors**
- **50V Rated output channels for long LED strings**
- **±1.5% (typ.) LED Current accuracy between channels**
- **±3% (typ.) LED Current accuracy between chips**
- **Standard DMX512 protocol decoder (USITT DMX512-A)**
- **4X DMX512 protocol selection (Baud rate=1MHz)**
- **Wide common-mode range for differential input signals**
- **Gamma, 2.2, to transform 8bits DMX to 14bits APDM data**
- **14bits grayscale resolution with Adaptive Pulse Density Modulation**
- **Frame refresh rate > 2000Hz as a LED driver**
  **Frame refresh rate > 120Hz as a PWM generator**
- **Traditional non-scramble constant current waveform for high power LED applications (PWM generator only)**
- **512 addresses set by 9 external pins**
- **Built-in oscillator for grayscale control and DMX512 decoder**
- **-40°C to +85°C Ambient temperature range**

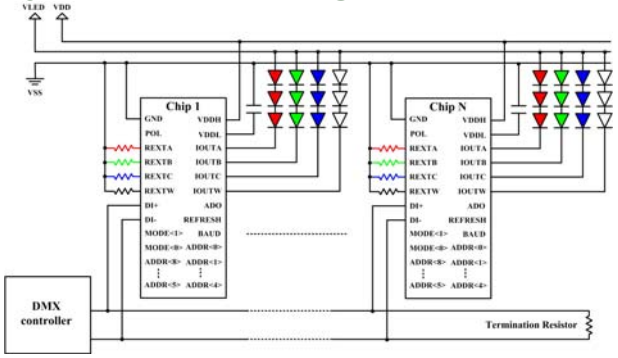
## Applications

- ❑ Standard DMX512 protocol system
- ❑ Full Color Mesh Display
- ❑ Architectural and Decorative Lighting

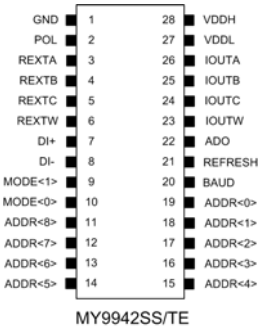
## Order information

| PART | PIN PACKAGE | |
|---|---|---|
| MY9942SS | SSOP28-150mil-0.635mm | 2500 pcs/Reel |
| MY9942TE | TSSOP28-173mil-0.65mm | 2500 pcs/Reel |

## Typical Operating Circuits




## Pin Configuration

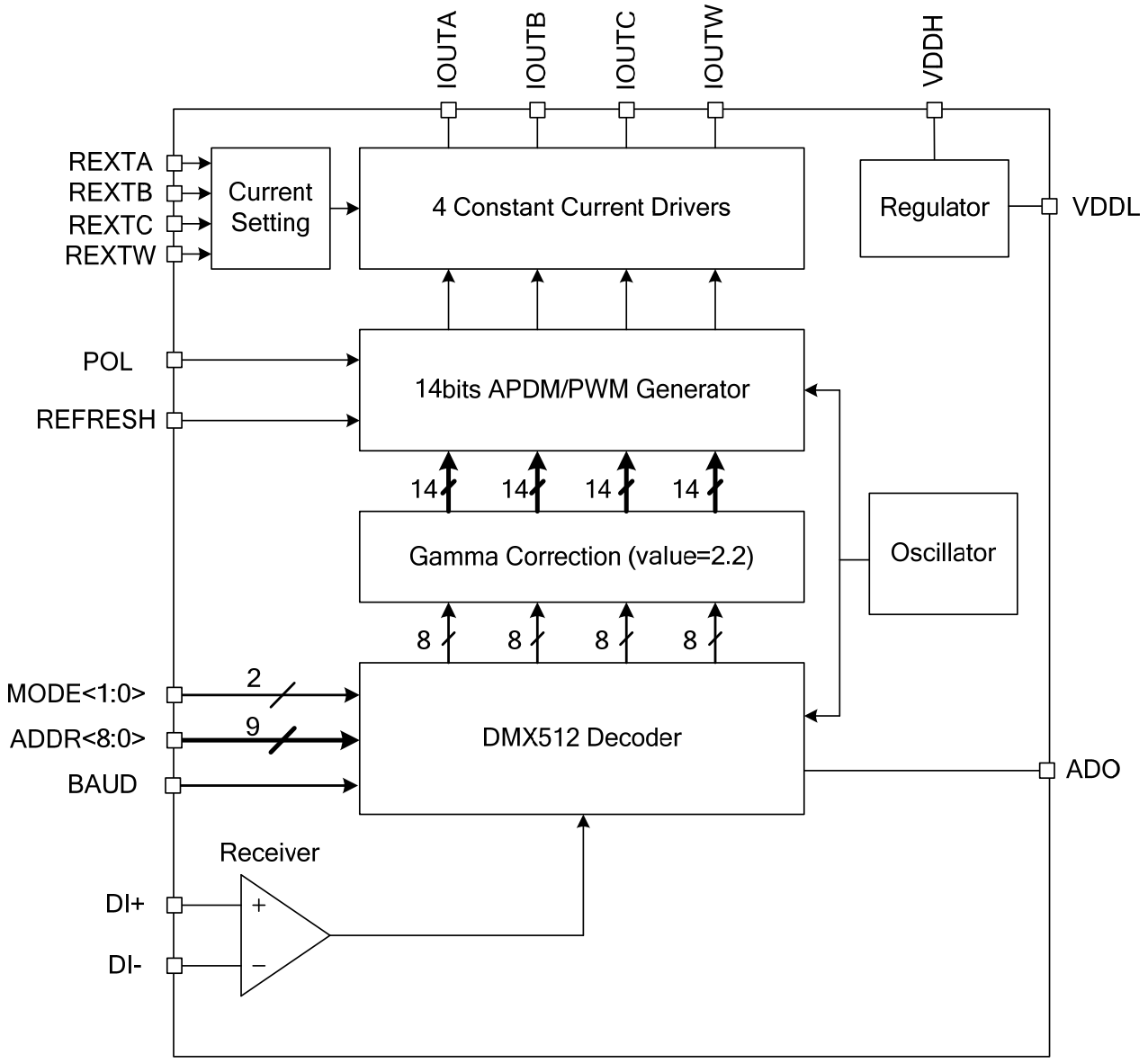



MY9942SS/TE



For pricing, delivery, and ordering information, pleases contact MY-Semi Inc. at +886-3-658-5656, or email to INFO@MY-Semi.com.tw or visit MY-Semi's website at www.MY-Semi.com.tw

## Block Diagram

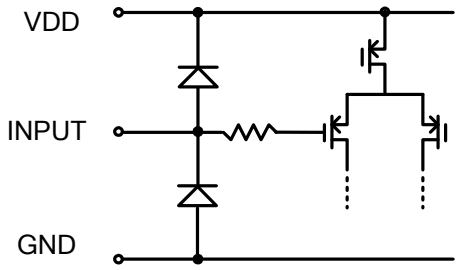


## Pin Assignment

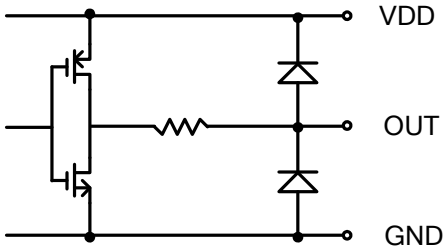
| IN No. TSSOP28 | PIN NAME | FUNCTION |
|---|---|---|
| 1 | GND | Ground terminal. |
| 2 | POL | Output current polarity selection:<br>“L” : work as a PWM generator (traditional non-scrambled waveform)<br>“H(floating)” : work as a LED driver (APDM waveform) |
| 3<br>4<br>5<br>6 | REXTA<br>REXTB<br>REXTC<br>REXTW | External resistors connected between REXT and GND for IOUTA, IOUTB, IOUTC and IOUTW output current value setting. |
| 7 | DI+ | Positive input terminal of differential DMX signal. |
| 8 | DI- | Negative input terminal of differential DMX signal. |
| 9 | MODE<1> | Slot data selection: (Please refer to pagexxx)<br>MODE<1:0>=L & L : four slots mode<br>MODE<1:0>=L & H(floating) : one slot mode<br>MODE<1:0>=H(floating) & L : two slots mode<br>MODE<1:0>=H(floating) & H(floating) : three slots mode |
| 10 | MODE<0> | |
| 11~19 | ADDR<8:0> | Address setting terminals |
| 20 | BAUD | DMX data rate selection:<br>“L” : 4 times DMX data rate (4x)<br>“H(floating)” : standard DMX data rate (1x) |
| 21 | REFRESH | Refresh rate selection (only for POL=”L”) :<br>“L” : refresh rate = 480Hz<br>“H(floating)” : refresh rate = 120Hz |
| 22 | ADO | Single-line addressing output terminal.<br>This pin could transmit an addressing signal to the ADI pin of next MY9943. |
| 23<br>24<br>25<br>26 | IOUTW<br>IOUTC<br>IOUTB<br>IOUTA | Output terminals for constant current output |
| 27 | VDDL | Voltage regulator output. Connecting a capacitor, 10uF, between VDDL pin and GND pin to stabilize the output voltage, 5V. |
| 28 | VDDH | Supply voltage terminal. |

## Equivalent Circuit of Inputs and Output

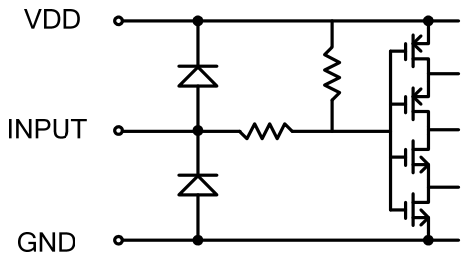
### 1. DI+, DI- terminals



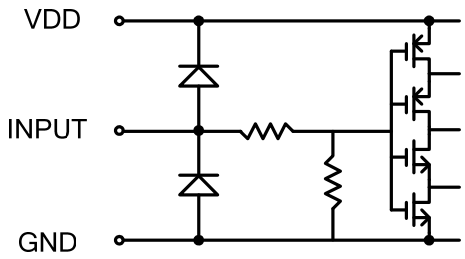

### 2. ADO terminals




### 3. POL, MODE<1:0>, REFRESH, BAUD terminals




### 4. ADDR<8:0> terminals




## Maximum Ratings (Ta=25°C, Tj(max) = 150°C)

| CHARACTERISTIC | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Supply Voltage | VDDH | 44 | V |
| Regulator Voltage | VDDL | 7 | V |
| Input Voltage | VIN | -0.3 ~ VDDL+0.3 | V |
| Output Current | IOUT | 370 | mA |
| Output Voltage | VOUT | -0.3 ~ 50 | V |
| Thermal Resistance (On PCB) | Rth(j-a) | 80 (SS:SSOP28-150mil-0.635mm ) | °C/W |
| | | 25 (TE:TSSOP28-173mil-0.65mm ) | |
| Operating Ambient Temperature | Top | -40 ~ 85 | °C |
| Storage Temperature | Tstg | -55 ~ 150 | °C |

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other condition beyond those specified is not supported.
(2) All voltage values are with respect to ground terminal.

## Electrical Characteristics (VDDL = 5.0 V, Ta = 25°C unless otherwise noted)

| CHARACTERISTIC | SYMBOL | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Differential Output voltage (Unloaded) | VOD1 | Io=0mA, figure 1 | | — | 5 | V |
| Differential Output voltage (loaded) | VOD2 | R=27Ω, figure 1 | 1.5 | — | 2 | |
| Differential Common-mode Output Voltage | VOC | R=27Ω, figure 1 | — | — | 3 | |
| Differential Input Threshold Voltage | VTH | -7V ≤VCM ≤ 12V | -0.2 | | 0.2 | |
| Differential Input Hysteresis | ΔVTH | VCM=0V | | 70 | | mV |
| Differential Input Resistance | RIN | | 192 | | | kΩ |
| Differential Output Short-Circuit Current, Vout=High | IOS1 | Vout=-7V | | | TBD | mA |
| Differential Output Short-Circuit Current, Vout=Low | IOS2 | Vout=10V | TBD | | | mA |
| Input Current of Differential Input | IDI | VIN=12V | | 50 | | uA |
| | | VIN=-7V | | -30 | | |
| Regulator Output Voltage | VDDL | VDDH=7~40V | | 5 | | V |
| Current Setting Feedback Voltage | Vrext | VDDH=40V Rrext=20Ω and Vo=1V | | 0.4 | | V |
| IOUT Leakage Current | ILK | Vo=48V | | | 0.1 | uA |
| Output Current Skew (Channel-to-Channel) *1 | dIOUT1 | VOUT = 1.0 V Rrext =16 Ω | — | ±1.5 | ±3 | % |
| Output Current Skew (Chip-to-Chip) *2 | dIOUT2 | | — | ±3 | ±6 | % |
| Output Current Skew (Channel-to-Channel) *1 | dIOUT1 | VOUT = 1.0 V Rrext =2.6 Ω | — | ±1.5 | ±3 | % |
| Output Current Skew (Chip-to-Chip) *2 | dIOUT2 | | — | ±3 | ±6 | % |
| Output Voltage Regulation*3 | % / VOUT | Rrext = 16 Ω VOUT = 7 V ~ 40 V | — | — | ±.0.1 | % / V |
| Supply Voltage Regulation*4 | % / VDDH | Rrext = 16Ω VDDH = 7 V ~ 40 V | — | ±0.6 | ±1 | |

*1 Channel-to-channel skew is defined by the formula below:

$$\Delta(\%) = \left[ \frac{Iout_n}{\frac{(Iout_0 + Iout_1 + \ldots + Iout_{15})}{16}} - 1 \right] * 100\%$$

*2 Chip-to-Chip skew is defined by the formula below:

$$\Delta(\%) = \left[ \left( \frac{\frac{(Iout_0 + Iout_1 + \ldots + Iout_{15})}{16} - (Ideal\ \ Output\ \ Current)}{(Ideal\ \ Output\ \ Current)} \right] * 100\%$$

*3 Output voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[ \frac{Iout_n(@Vout_n = 3V) - Iout_n(@Vout_n = 1V)}{Iout_n(@Vout_n = 3V)} \right] * \frac{100\%}{3V - 1V}$$

*4 Supply voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[ \frac{Iout_n(@V_{DDH} = 40V) - Iout_n(@V_{DDH} = 7V)}{Iout_n(@V_{DD} = 7V)} \right] * \frac{100\%}{40V - 7V}$$

| CHARACTERISTIC | SYMBOL | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Supply Current | $I_{DD1(off)}$ | all pins are open unless VDD and GND | — | 1.7 | 2.5 | mA |
| | $I_{DD2(off)}$ | input signal is static Rrext = 16 Ω all outputs turn off | — | 2.3 | 3.1 | |
| | $I_{DD1(on)}$ | input signal is static Rrext = 16 Ω all outputs turn on | — | 2.4 | 3.2 | |
| | $I_{DD3(off)}$ | input signal is static Rrext = 2.6 Ω all outputs turn off | — | 6.0 | 6.5 | |
| | $I_{DD2(on)}$ | input signal is static Rrext = 2.6 Ω all outputs turn on | — | 6.1 | 6.6 | |

## Switching Characteristics (VDDL = 5.0V, Ta = 25°C unless otherwise noted)

| CHARACTERISTIC | SYMBOL | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Propagation Delay From DI to DO ( “L” to “H” ) | tpLH | VDDH=40V $R_{DIFF}$=54Ω $R_{LOAD}$=196kΩ $C_L$=100pF DI(diff)=1.5V | — | 40 | | ns |
| Propagation Delay From DI to DO ( “H” to “L” ) | tpHL | | — | 40 | | |
| Propagation Delay Skew | tskew | | | 5 | | |
| DO rise time | $tr_{(DO)}$ | | — | 20 | | |
| DO fall time | $tf_{(DO)}$ | | | 20 | | |
| Output Current Rise Time | tor | | 100 | | | |
| Output Current Fall Time | tof | — | 100 | — | | |
| Internal Grayscale Clock Frequency | FGCK | | | 2 | | MHz |

## Test Circuits

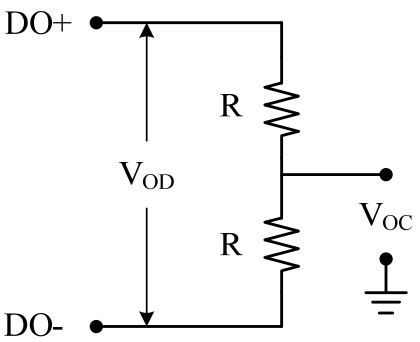



**Figure1. Differential Output DC Test Circuit**

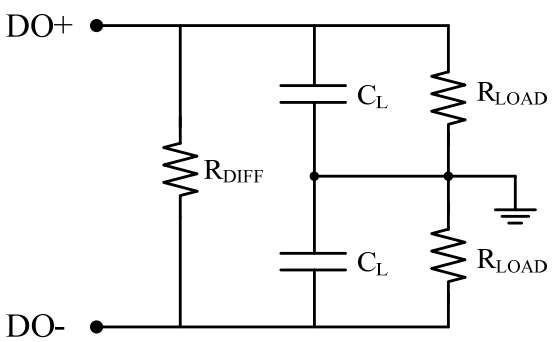



**Figure2. Differential Output Timing Test Circuit**

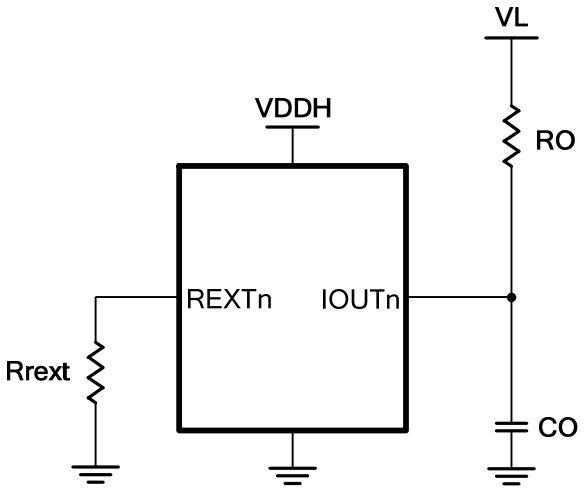
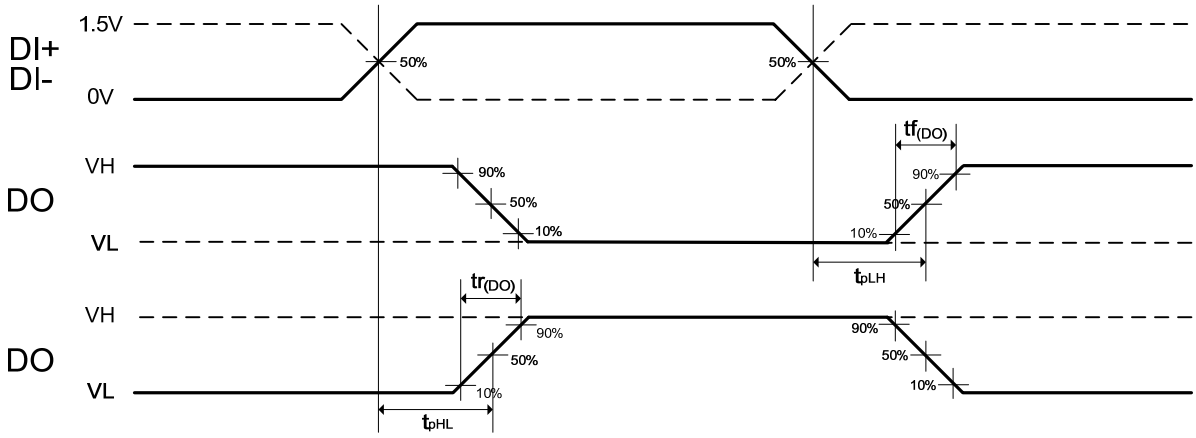


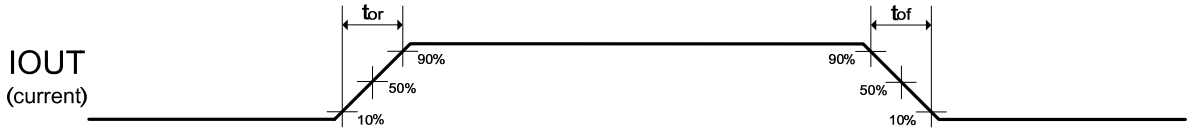

**Figure3. IOUT Switching Characteristics Test Circuit**

## Timing Diagram

1. DI to DO




2. IOUT

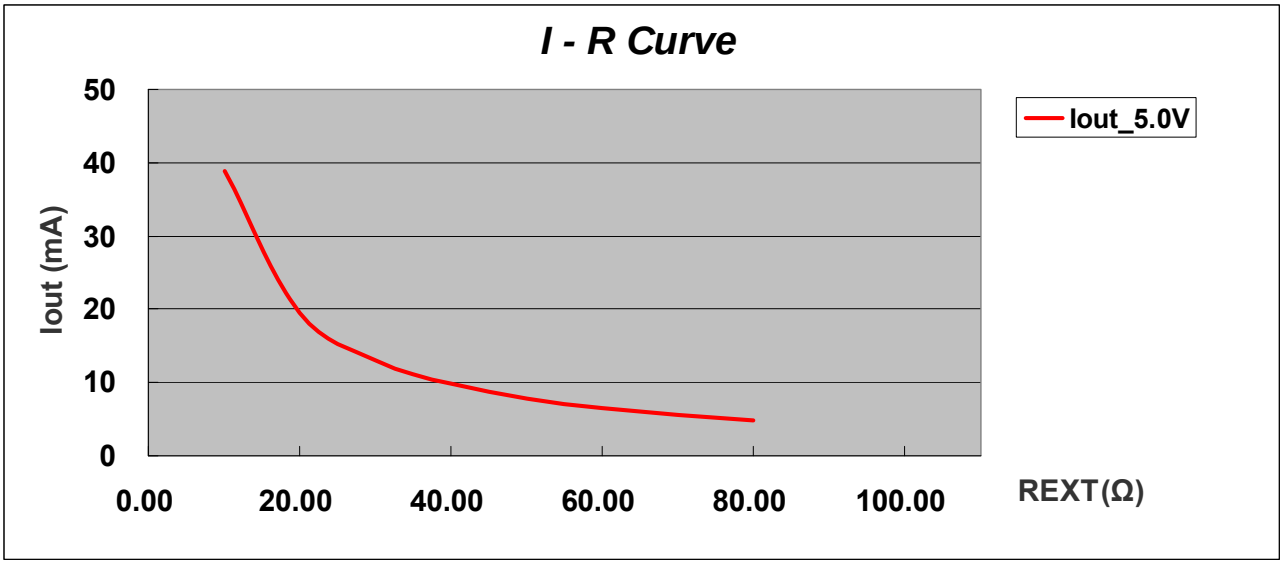


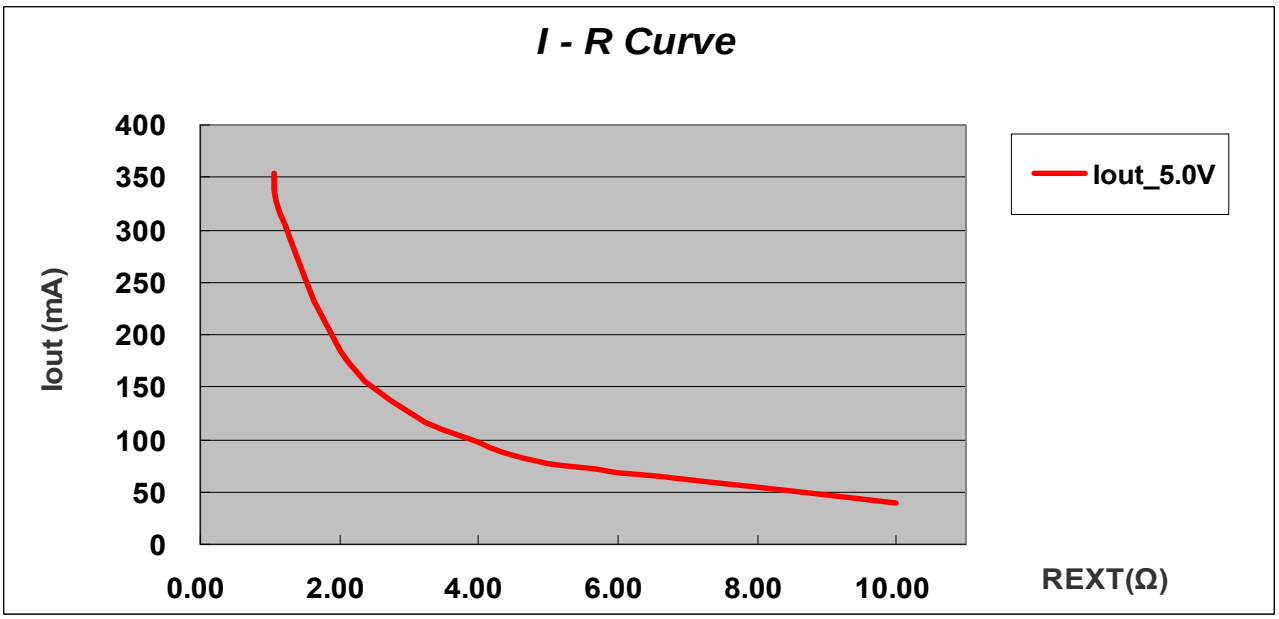
## Reference Resistor

The constant current values are determined by an external resistor placed between REXT pin and GND pin. The following formula is utilized to calculate the current value:

$$Iout(mA)=Vrext(V) / Rext(k\Omega) = 0.4V / Rext(k\Omega)$$

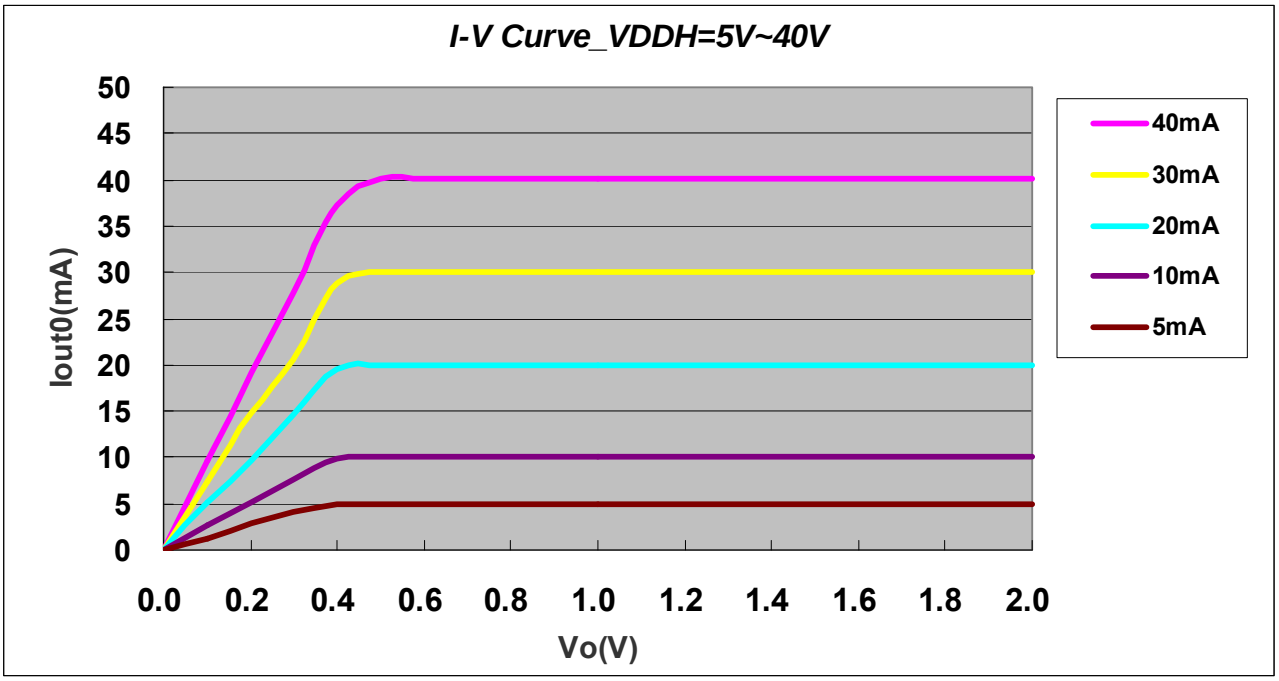
Where Rrext is a resistor placed between REXT and GND
For example, Iout is 20mA when Rrext=20Ω and Iout is 50mA when Rrext=8 Ω

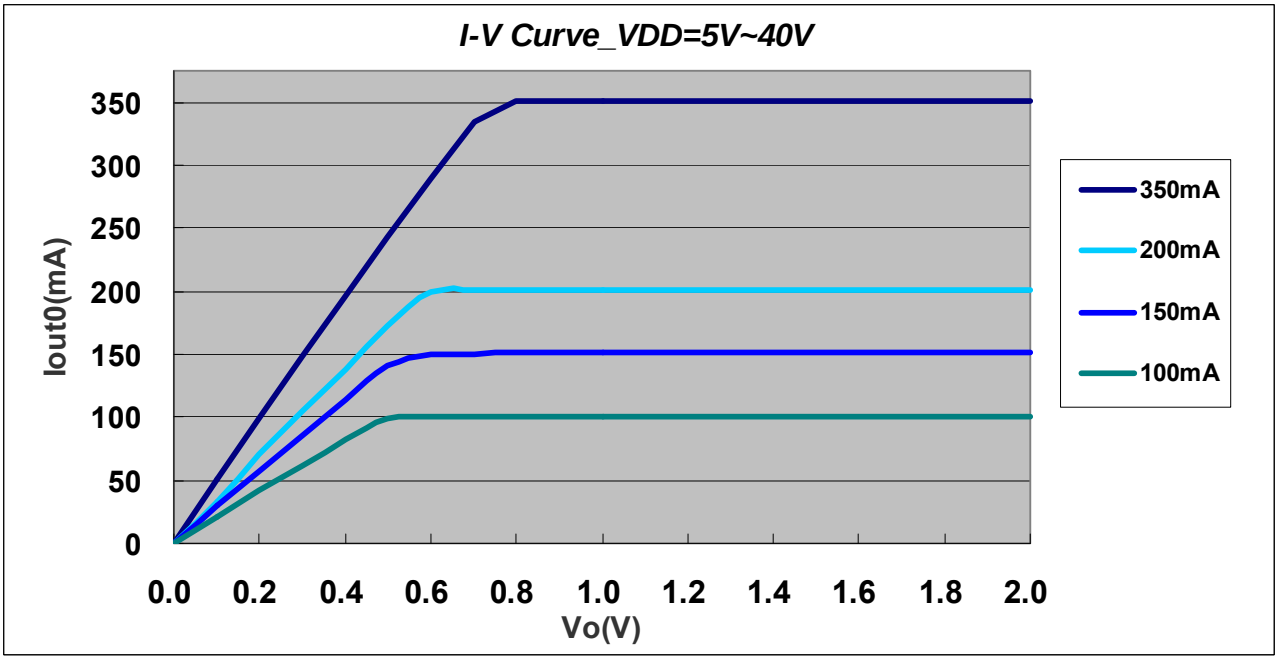


## Constant-Current Output

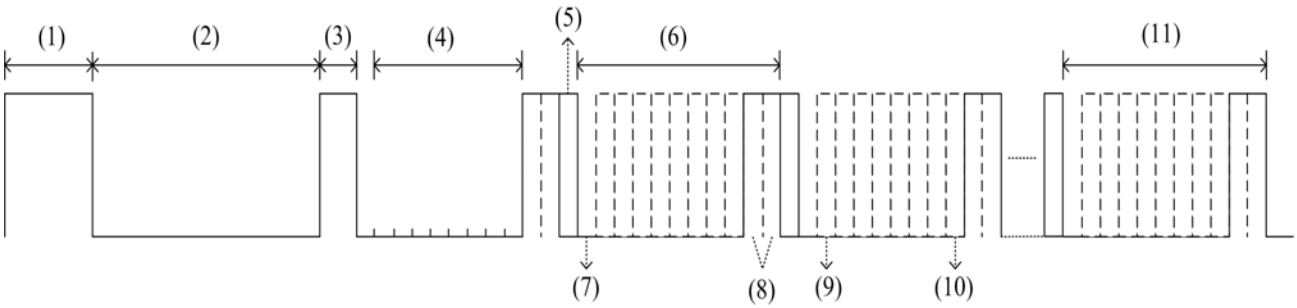
The current characteristics could maintain invariable in the influence of loading voltage. Therefore, the MY9942 could minimize the interference of different LED forward voltages and produce the constant current. The following figures illustrate the suitable output voltage should be determined in order to keep an excellent performance.



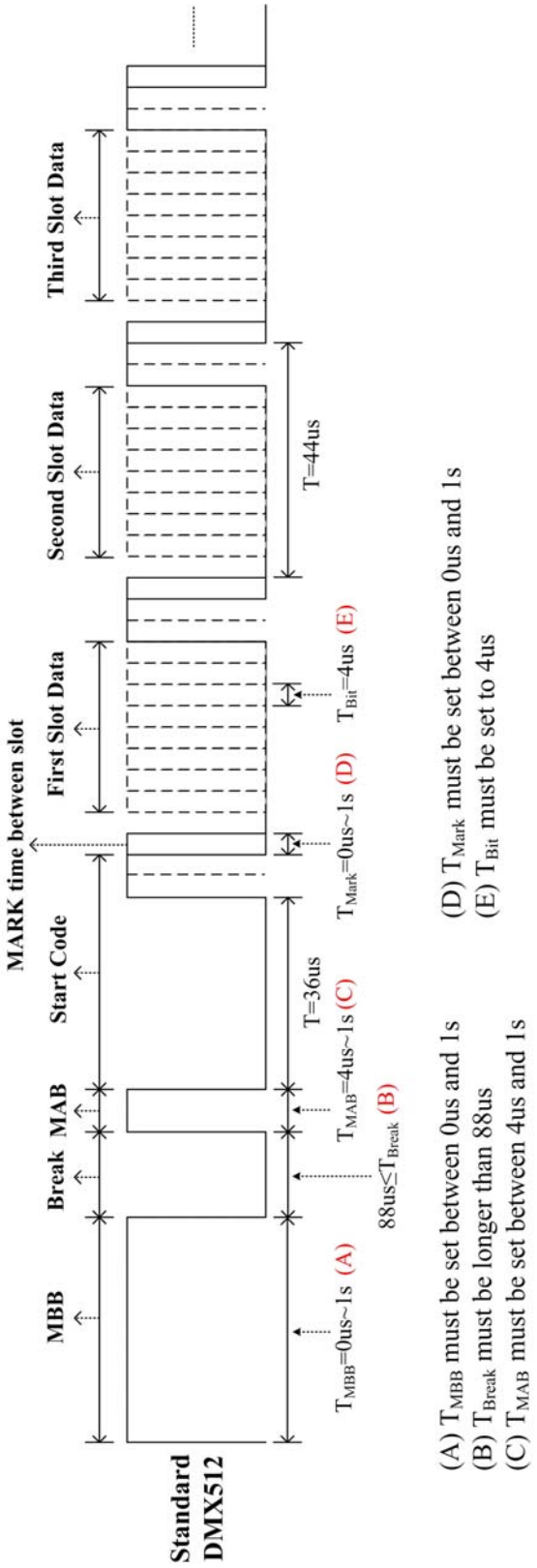
## Standard USITT DM512-A Protocol (BAUD=H/floating)

DMX512 is a standard that describes a method of digital data transmission between controllers and lighting equipment and accessories. MY9942 completely supports DMX512 protocol in accordance with USITT DMX512-A standard.



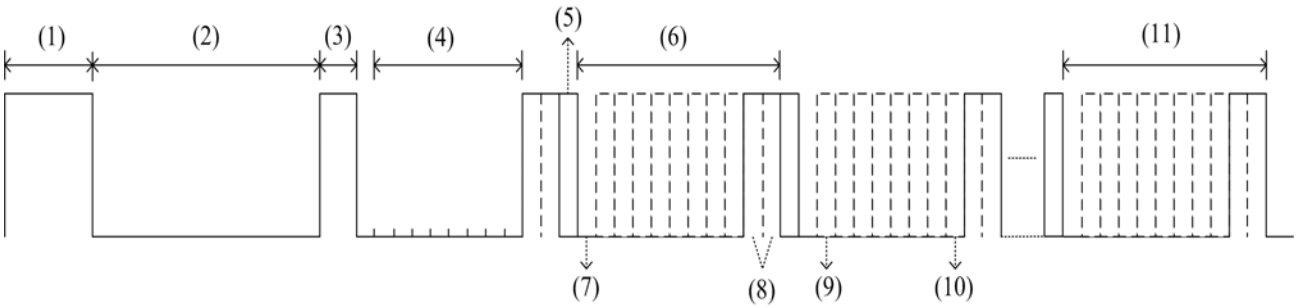

| Reference | Description | Duration |
|---|---|---|
| (1) | Mark Time Before Break (MBB) | 0us~1s |
| (2) | Break | ≧88us |
| (3) | Mark Time After Break (MAB) | 4us~1s |
| (4) | Start Code (Slot 0 data) | 32us ± 2%<br>(Start Code must be null) |
| (5) | Mark Time Between Slot | 0s~1s |
| (6) | Slot Time | 44us ± 2% |
| (7) | Start Bit | 4us ± 2% |
| (8) | Stop Bits | 4us ± 2% |
| (9) | Least Significant Data Bit | 4us ± 2% |
| (10) | Most Significant Data Bit | 4us ± 2% |
| (11) | The Number of Slots | Not Limited |

## Standard DMX512 Interface



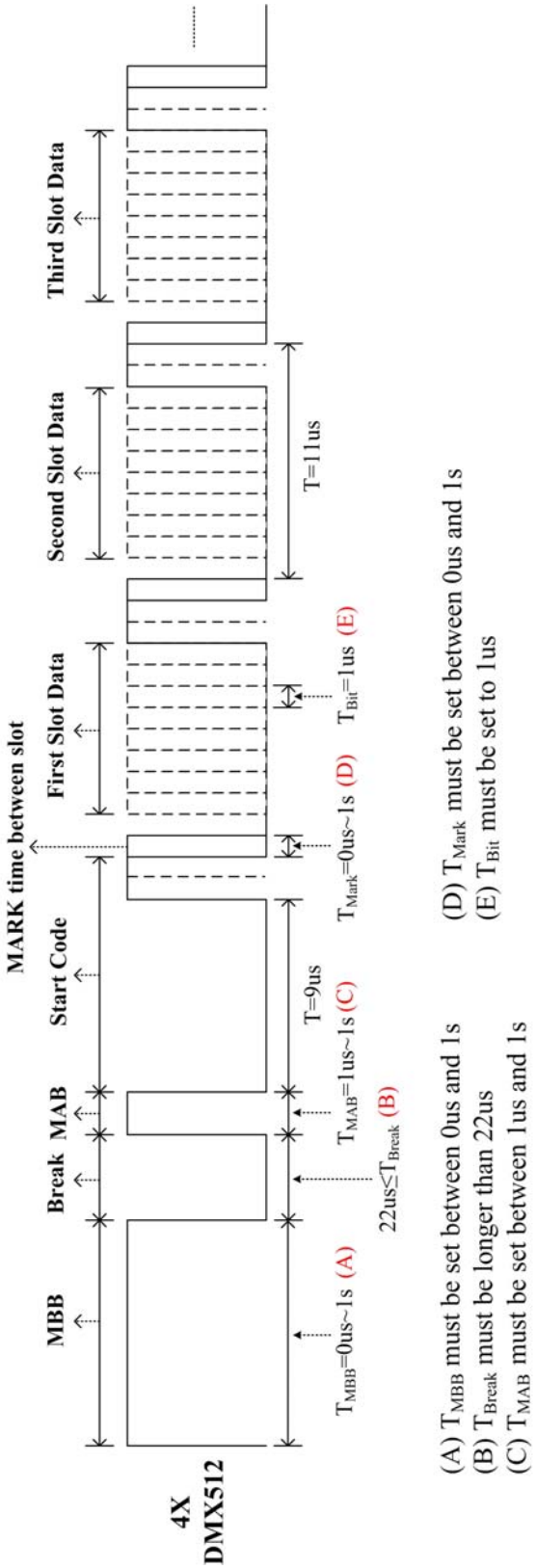
## 4X DM512 Protocol (BAUD=L)

DMX512 is a standard that describes a method of digital data transmission between controllers and lighting equipment and accessories. MY9942 also supports 4X DMX512 protocol in order to enhance data refresh rate.

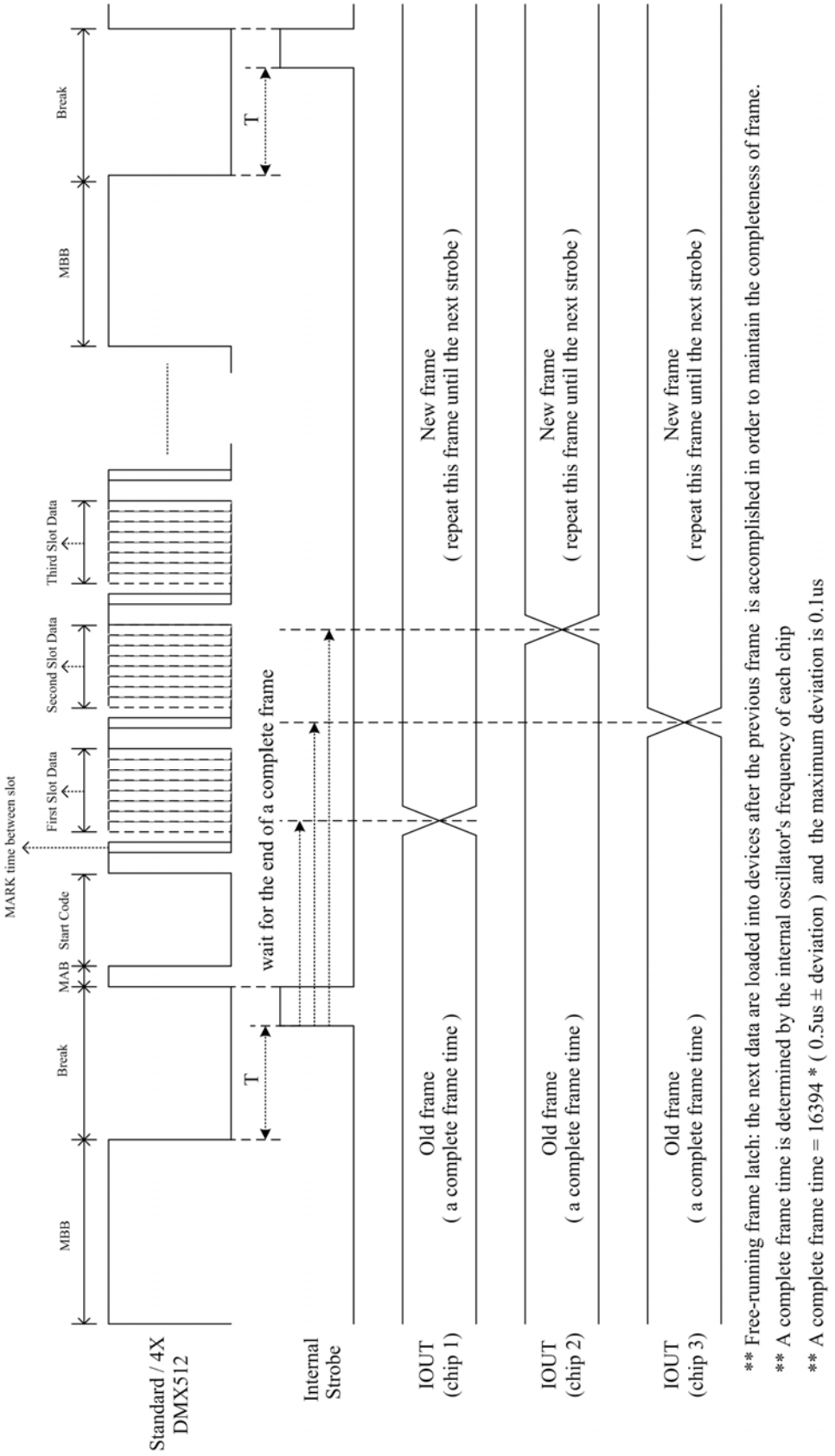



| Reference | Description | Duration |
|---|---|---|
| (1) | Mark Time Before Break (MBB) | 0us~1s |
| (2) | Break | ≧22us |
| (3) | Mark Time After Break (MAB) | 1us~1s |
| (4) | Start Code (Slot 0 data) | 8us ± 2%<br>(Start Code must be null) |
| (5) | Mark Time Between Slot | 0s~1s |
| (6) | Slot Time | 11us ± 2% |
| (7) | Start Bit | 1us ± 2% |
| (8) | Stop Bits | 1us ± 2% |
| (9) | Least Significant Data Bit | 1us ± 2% |
| (10) | Most Significant Data Bit | 1us ± 2% |
| (11) | The Number of Slots | Not Limited |

## 4X DMX512 Interface



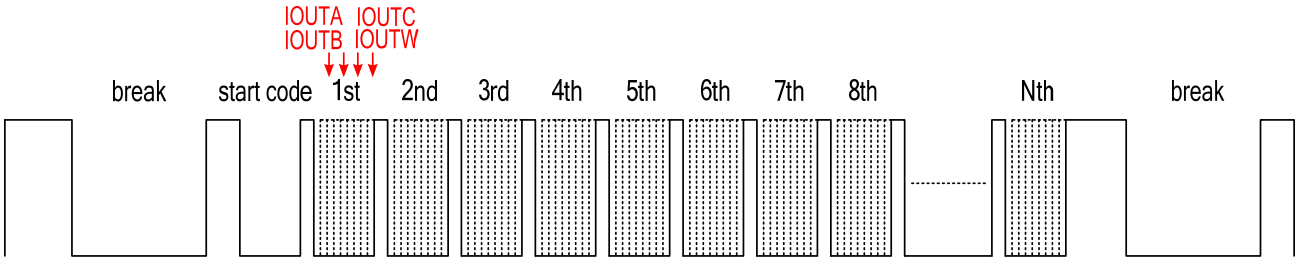
## Frame Latch (Break)



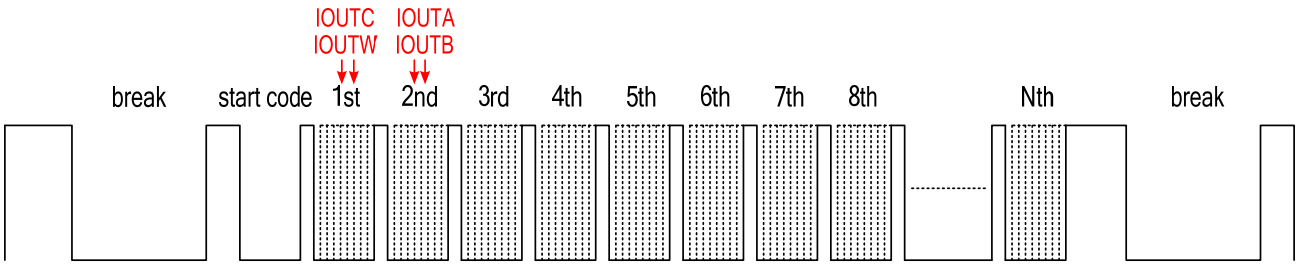
## Slot Data Selection ( ADDR<8:0>= 0 0000 0000 )

MY9942 loads grayscale data according to two slot selection pins (MODE<1:0>) and nine address setting pins. For example, MY9942 would loads slots data illustrated below when nine address setting pins ADDR<8:0> are 0 0000 0000.

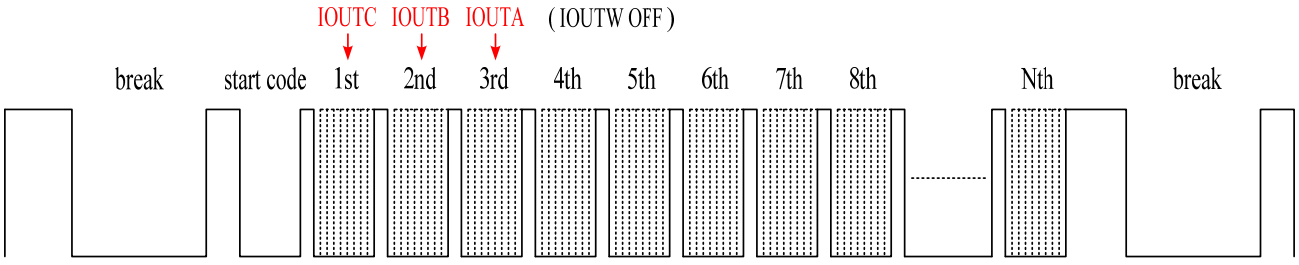
**MODE<1> : MODE<0> = L : H ➔ One slot mode**



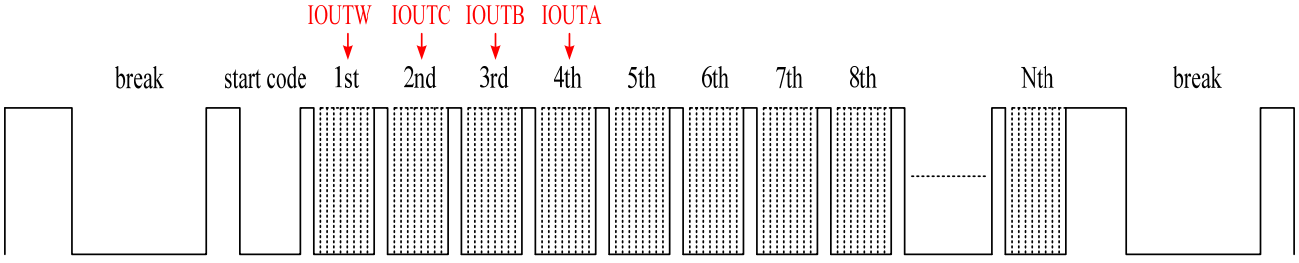

**MODE<1> : MODE<0> = H : L ➔ Two slots mode**




**MODE<1> : MODE<0> = H : H ➔ Three slots mode**



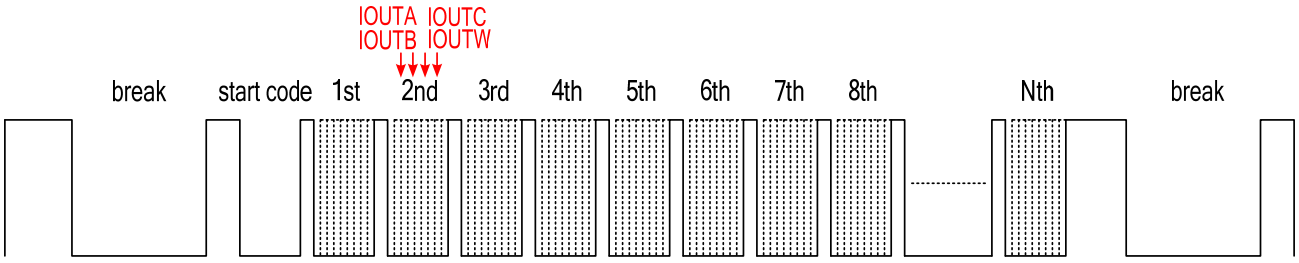

**MODE<1> : MODE <0> = L : L ➔ Four slots mode**



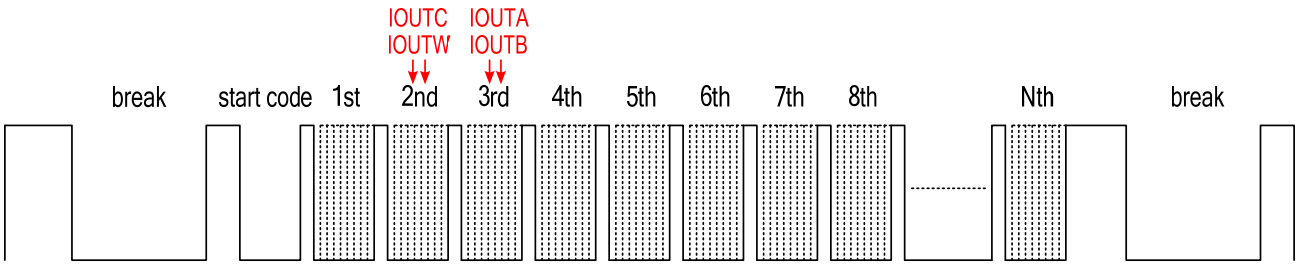
## Slot Data Selection ( ADDR<8:0>= 0 0000 0001)

MY9942 loads grayscale data according to two slot selection pins (MODE<1:0>) and nine address setting pins. For example, MY9942 would loads slots data illustrated below when nine address setting pins ADDR<8:0> are 0 0000 0001.

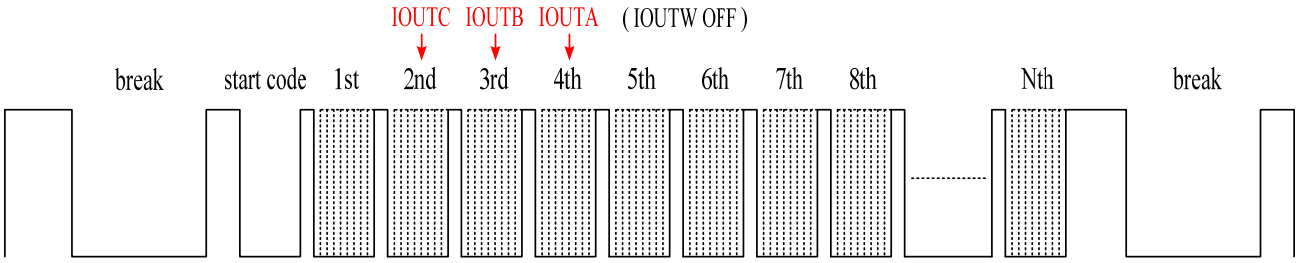
**MODE<1> : MODE<0> = L : H ➔ One slot mode**



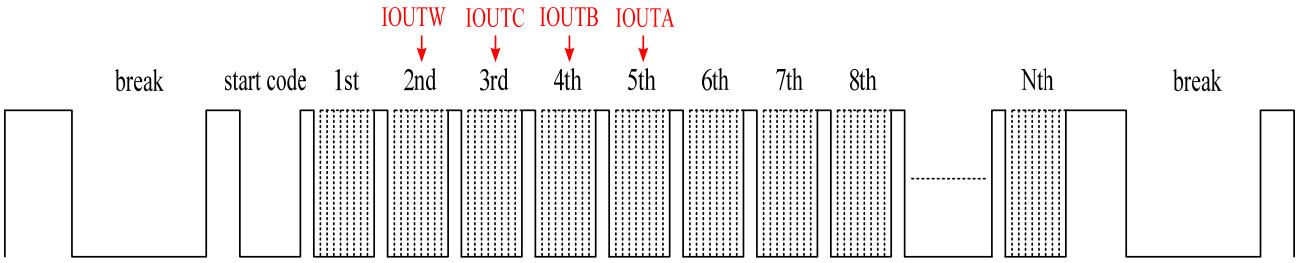

**MODE<1> : MODE<0> = H : L ➔ Two slots mode**



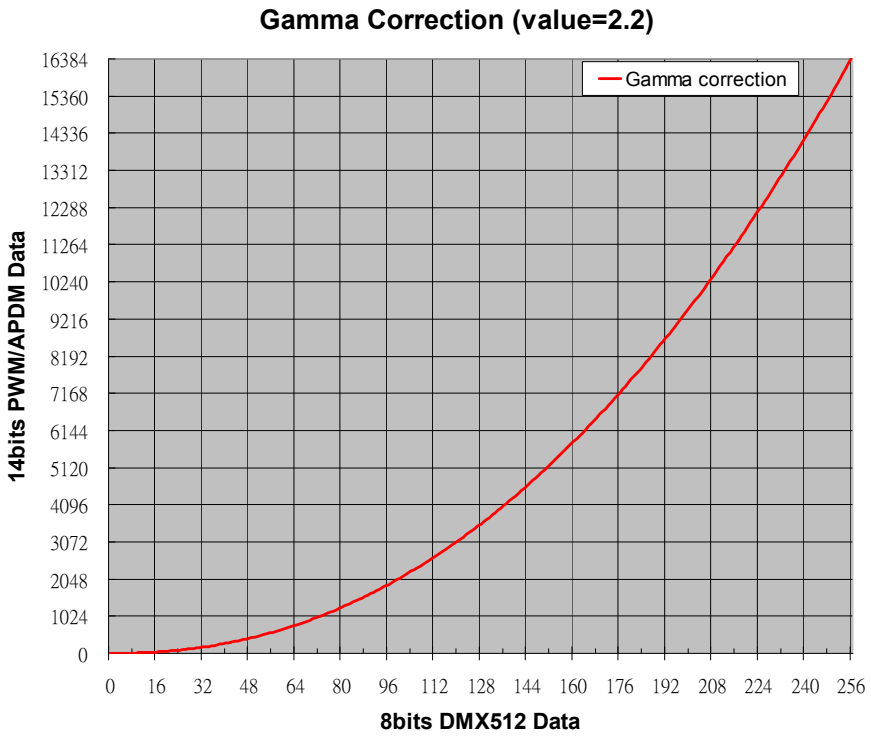

**MODE<1> : MODE<0> = H : H ➔ Three slots mode**




**MODE<1> : MODE<0> = L : L ➔ Four slots mode**

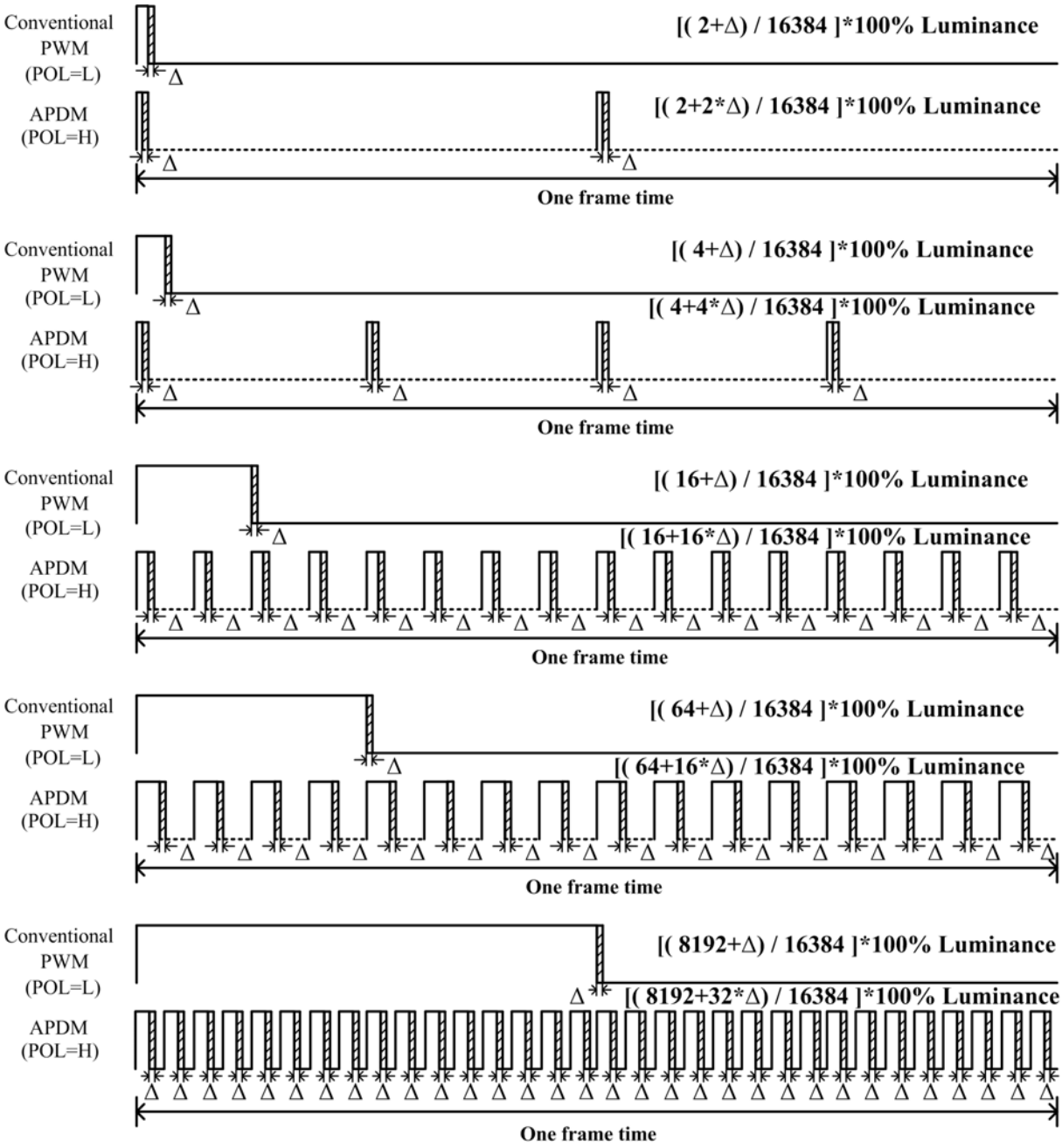


## Gamma Correction



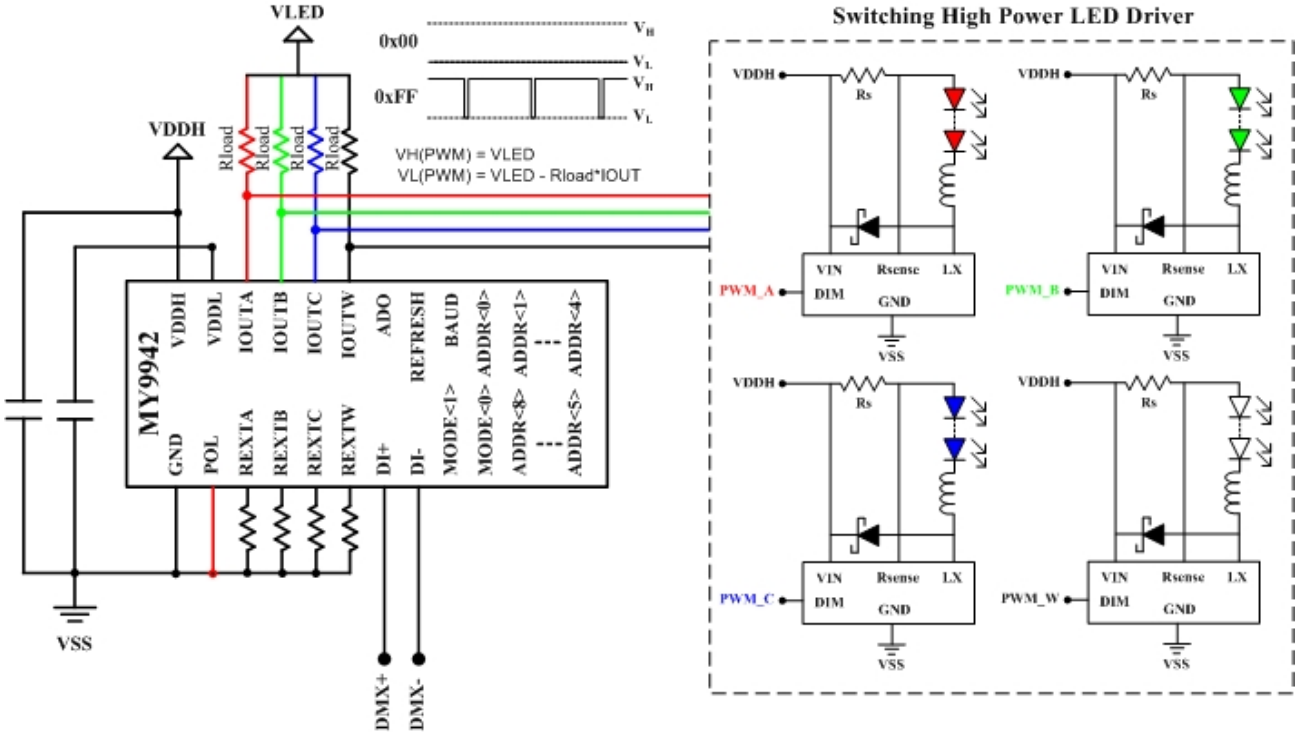

MY9942 supports Gamma Correction function, 2.2, to transform 8bits DMX512 data to 14bits PWM/APDM data in order to enhance brightness contract.

## APDM (Adaptive Pulse Width Modulation, only for LED driver, POL=H)



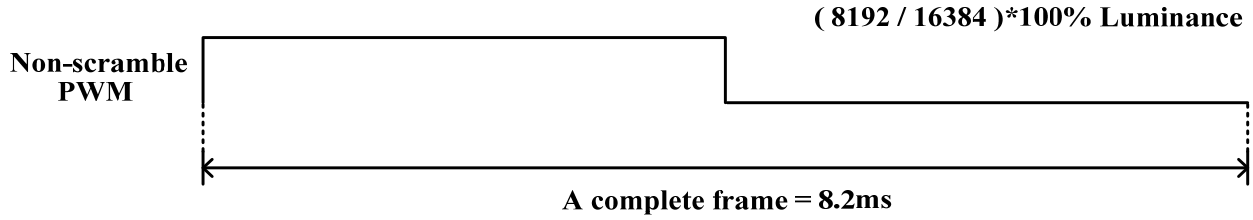

- ▲ The waveform is divided into 16 sections when the luminance is below 8192/16384.
- ▲ The waveform is divided into 32 sections when the luminance is over 8192/16384.
- ▲ MY-semi issues this APDM approach, Adaptive Pulse Width Modulation, in order to abate the non-ideal IOUT distortion due to non-symmetrical transient response at low luminance and improve the refresh rate at high luminance.
- ▲ The Δ-width correction technique (Δ≠0) is used to compensate the non-ideal output current transient response.

## PWM generator solution (POL=L)

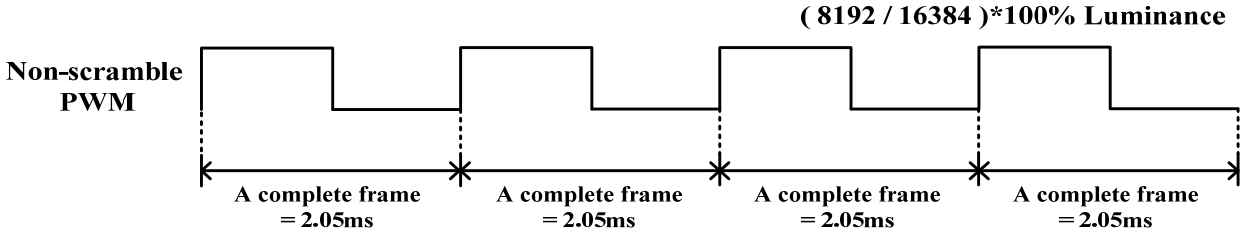



MY9942 could be set as a PWM generator to produce 14bits traditional non-scrambled PWM waveform for high power LED lighting applications. The POL pin is set to VSS and the IOUT pins are connected to VLED by Rload resistors in order to determine VH and VL level of PWM signal. Furthermore, MY9942 supports refresh rate selection function to set refresh rate as 120Hz or 480Hz.

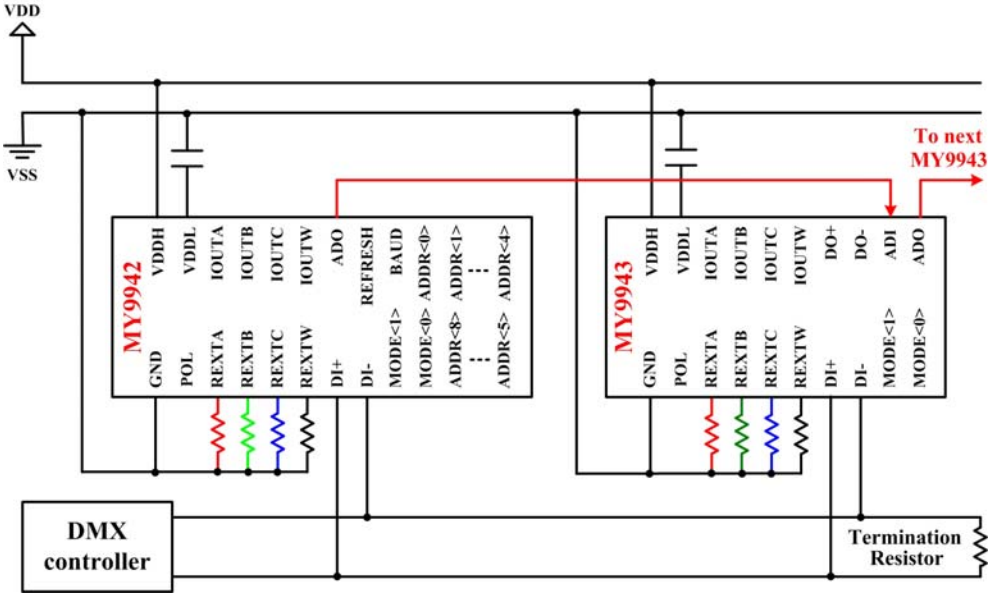
**REFRESH = H(floating) ➔ refresh rate = 120Hz (Grayscale clock=2MHz)**




**REFRESH = L ➔ refresh rate = 480Hz (Grayscale clock=8MHz)**

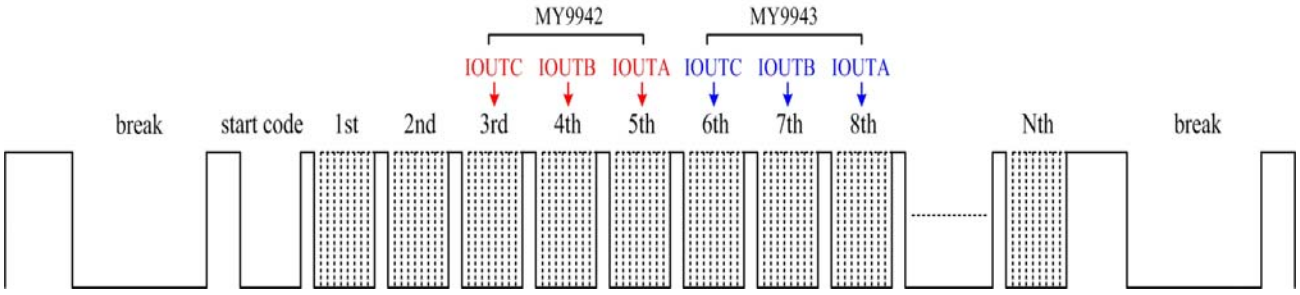


## Multi-channels solution (MY9942 + Single-line addressing MY9943)

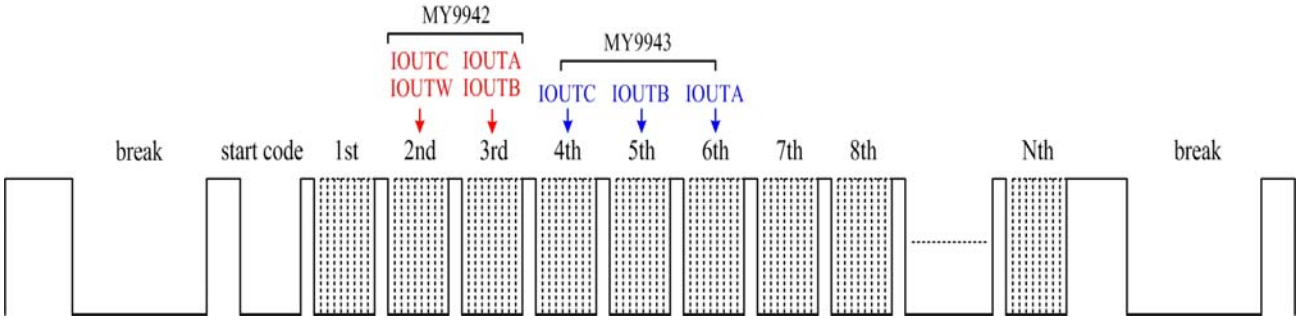



MY9942 could utilize the automatic addressing output pin, ADO, to control single-line addressing MY9943 in order to decrease the amount of addressing switches and reduce the complexity of lighting assembly. This solution utilizes ADDR<8:0> of MY9942 to set the initial position of DMX512 data loading and connect the ADO pin of MY9942 to the ADI pin of next MY9943. The sequence of data loading is illustrated below.

**Ex 1. ADDR<8:0> = 9'b0 0000 0010，Three slots mode(MY9942/MY9943)**

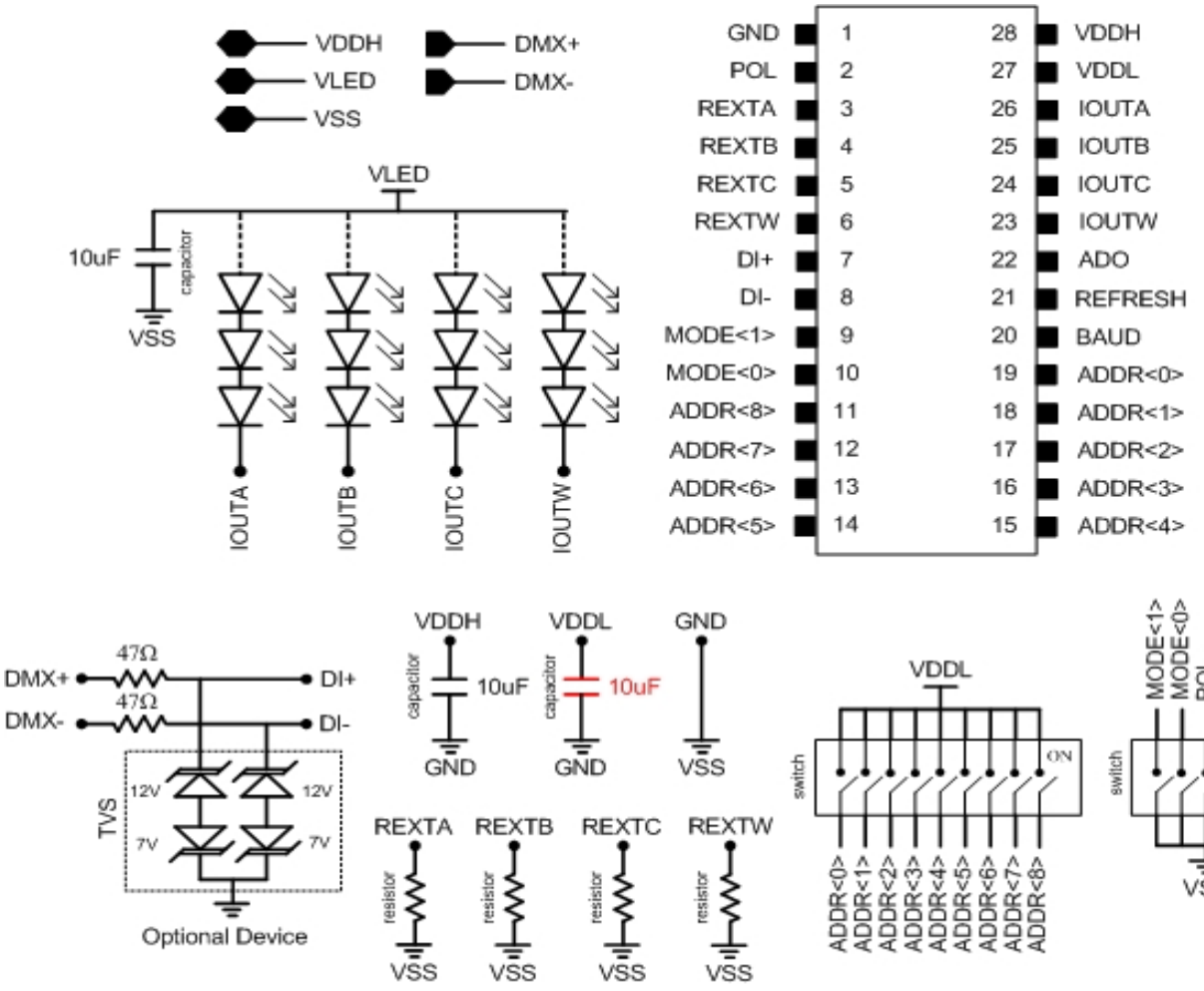



**Ex 2. ADDR<8:0> = 9'b0 0000 0001，Two slots mode(MY9942)，Three slots mode(MY9943)**



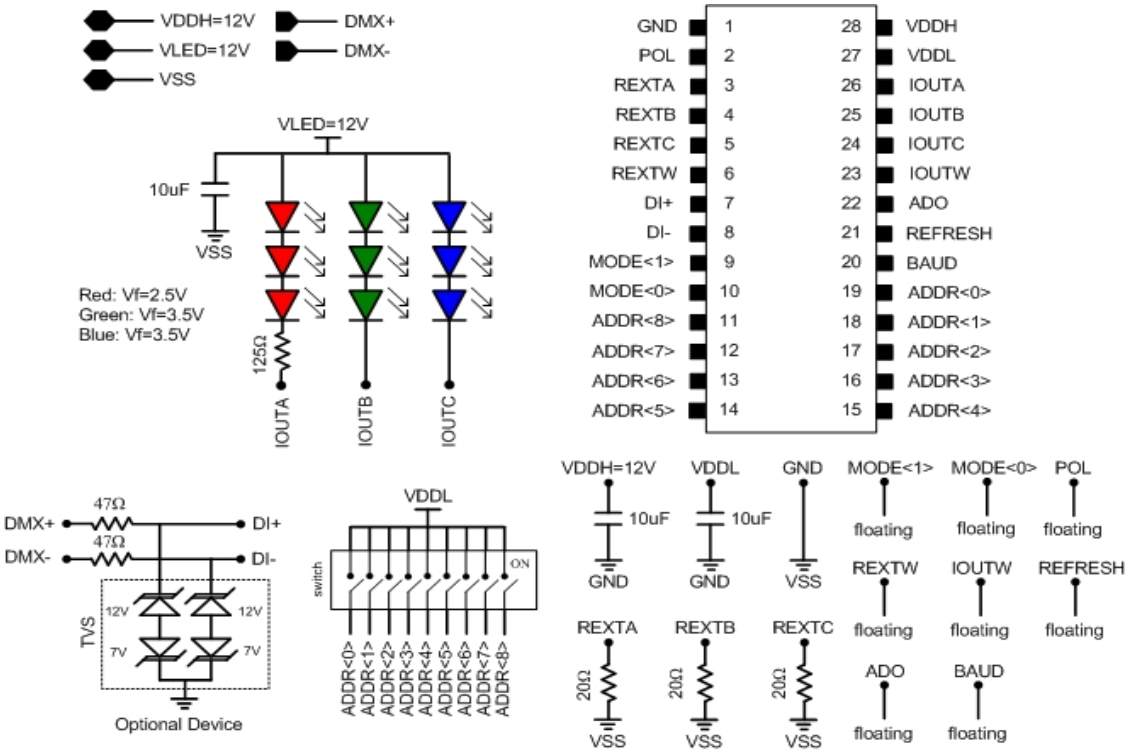
## Application (LED Driver)

VDDH=7V~40V

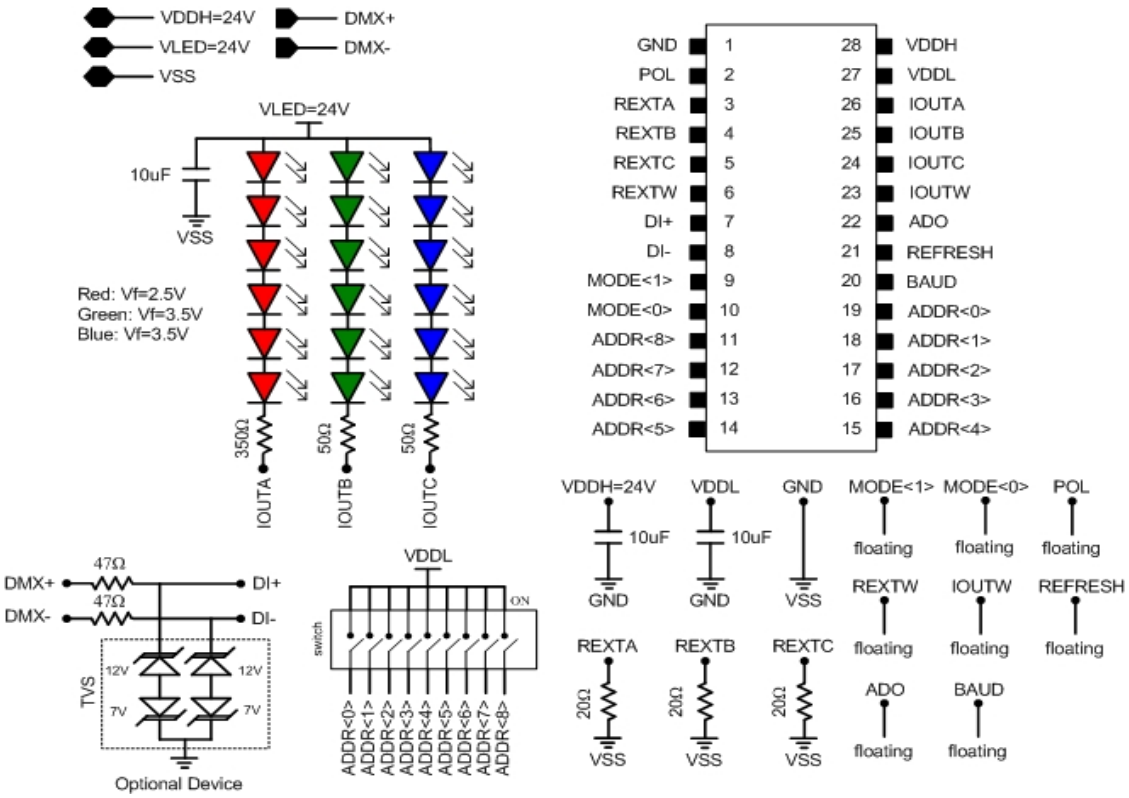


## Application Sample (LED Driver)

VDDH=VLED=12V, IOUT=20mA, Three slots mode, Standard DMX512 protocol

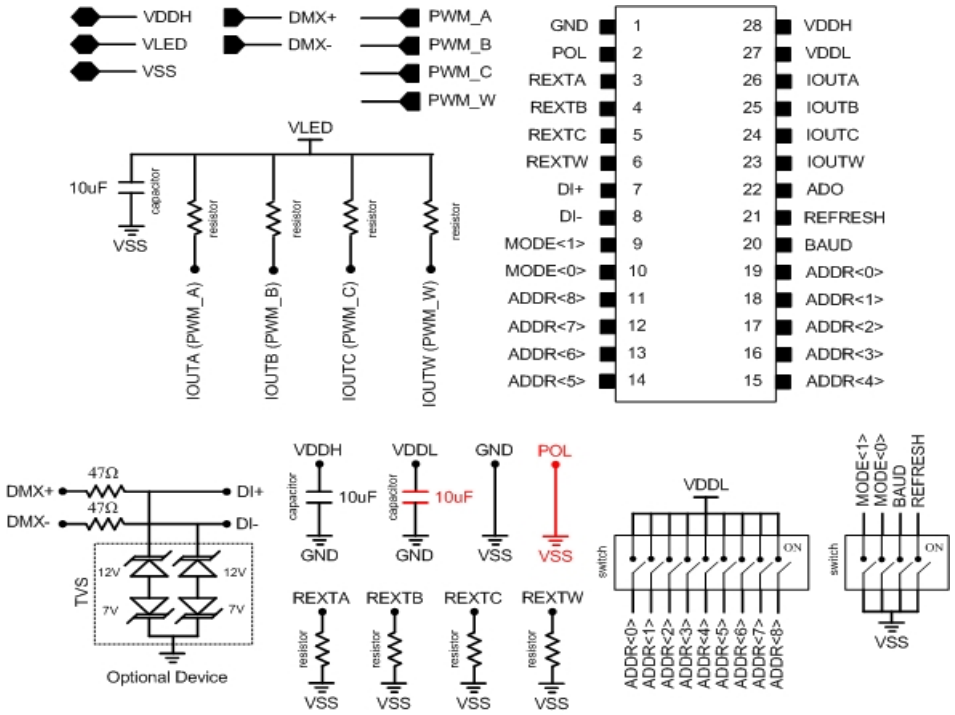



VDDH=VLED=24V, IOUT=20mA, Three slots mode, Standard DMX512 protocol



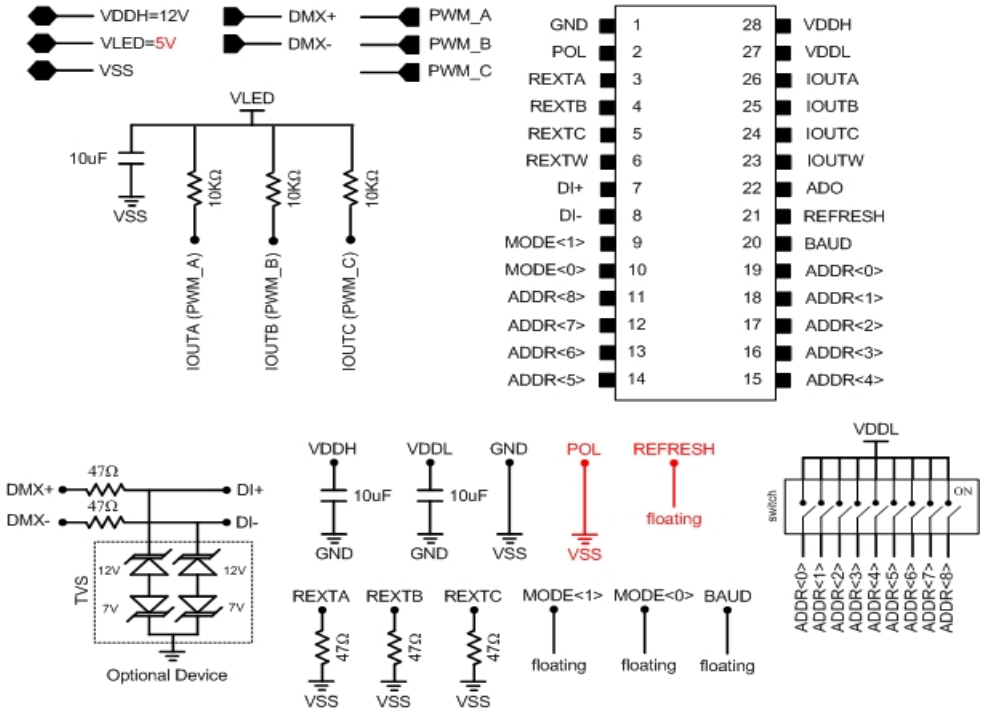
## Application (PWM Generator)

VDDH=7V~40V




## Application Sample (PWM Generator)

VDDH=12V,Refresh rate=120Hz, VH(PWM)=5V, VL(PWM)=0V, Standard DMX512 protocol



## Power Dissipation

When all four output channels are turned on, the practical power dissipation is determined by the following equation:

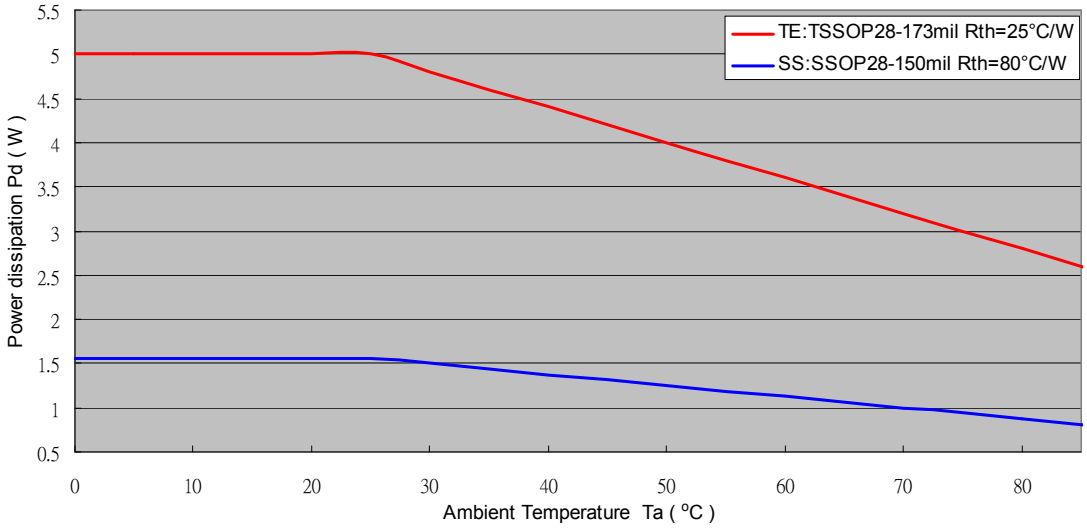
$$PD\ (practical) = V_{DDH} \times I_{DDH} + VoutA \times IoutA \times DutyA + VoutB \times IoutB \times DutyB + VoutC \times IoutC \times DutyC + VoutW \times IoutW \times DutyW$$

In secure operating conditions, the power consumption of an integrated chip should be less than the maximum permissible power dissipation which is determined by the package type and ambient temperature. The formula for maximum power dissipation is described as follows:

$$PD\ (max) = \frac{Tj(max)(℃) - Ta(℃)}{Rth(j\text{-}a)(℃/Watt)}$$

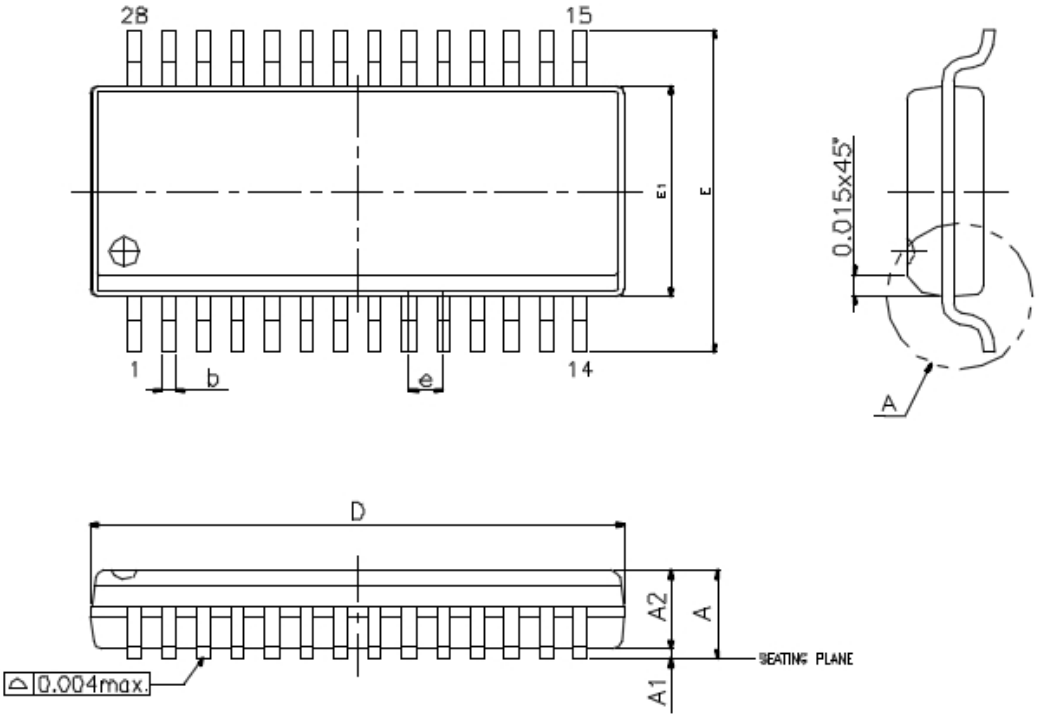
The PD(max) declines as the ambient temperature raises. Therefore, suitable operating conditions should be designed with caution according to the chosen package and the ambient temperature. The following figure illustrates the relation between the maximum power dissipation and the ambient temperature in the SSOP/TSSOP28 package.

Maximum Power Dissipation v.s. Ambient Temperature



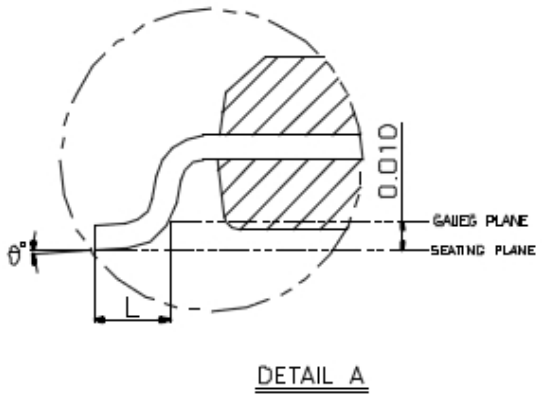
## Package Outline Dimension

SSOP28-150mil-0.635mm




| SYMBOLS | MIN. | MAX. |
|---|---|---|
| A | 0.053 | 0.069 |
| A1 | 0.004 | 0.010 |
| A2 | — | 0.059 |
| b | 0.008 | 0.012 |
| D | 0.386 | 0.394 |
| E1 | 0.150 | 0.157 |
| e | 0.025 BASIC | |
| E | 0.228 | 0.244 |
| L | 0.016 | 0.050 |
| θ° | 0 | 8 |

UNIT : INCH

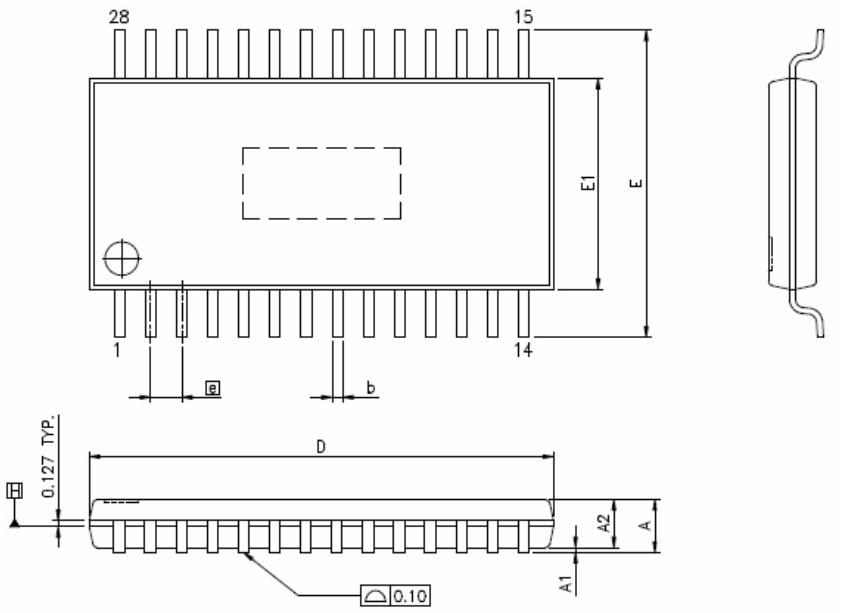


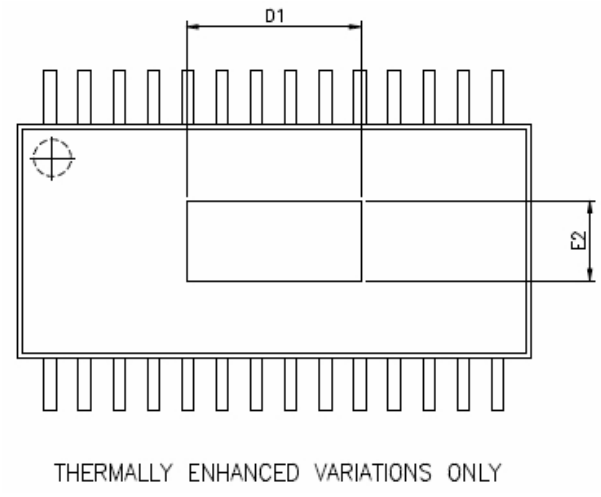

DETAIL A

NOTES:
1.JEDEC OUTLINE : MO-137 AF
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm (0.006in) PER SIDE.
3.DIMENSIONS "E1" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm (0.010in) PER SIDE.

## Package Outline Dimension

TSSOP28-173mil-0.65mm



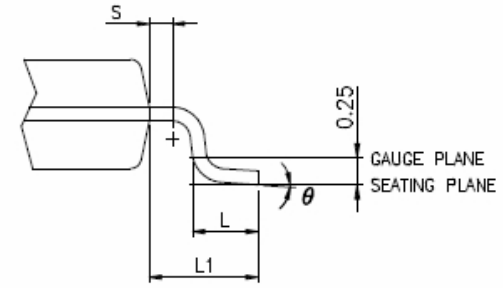




VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

| SYMBOLS | MIN. | NOM. | MAX. |
|---|---|---|---|
| A | – | – | 1.20 |
| A1 | 0.00 | – | 0.15 |
| A2 | 0.80 | 1.00 | 1.05 |
| b | 0.19 | – | 0.30 |
| D | 9.60 | 9.70 | 9.80 |
| E1 | 4.30 | 4.40 | 4.50 |
| E | 6.40 BSC | | |
| e | 0.65 BSC | | |
| L1 | 1.00 REF | | |
| L | 0.45 | 0.60 | 0.75 |
| S | 0.20 | – | – |
| θ | 0° | – | 8° |

THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

| PAD SIZE | E2 | | D1 | |
|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. |
| 118X21E | 2.40 | 3.00 | 4.41 | 5.51 |




NOTES:

1. JEDEC OUTLINE :
   STANDARD : MO-153 AE REV.F
   THERMALLY ENHANCED : MO-153 AET REV.F
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5. DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H .

The products listed herein are designed for ordinary electronic applications, such as electrical appliances, audio-visual equipment, communications devices and so on. Hence, it is advisable that the devices should not be used in medical instruments, surgical implants, aerospace machinery, nuclear power control systems, disaster/crime-prevention equipment and the like. Misusing those products may directly or indirectly endanger human life, or cause injury and property loss.
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